

Jinyoung Choi

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EDUCATION

UC RIVERSIDE	Computer Science and Engineering	Ph.D. 9/2019 - present
Soongsil University	Electronic Engineering	M.S. 3/2012 – 2/2014
	Thesis Title: A response time analysis and synthesis of motion applications in EtherCAT-based distributed real-time systems	
	Advisor: Kanghee Kim, Ph.D.	
Soongsil University	Electronic Engineering	B.S. 3/2008 – 2/2012

SKILL SET & KNOWLEDGE

- C/C++, CUDA, HIP, OpenCL, ROCm, Xilinx SDK, Linux Kernel, Git, JTAG, GDB.
- LLVM/LLVM-IR, Deep Learning algorithms/operations.

EXPERIENCE

Research Assistant, UC Riverside, Riverside, CA (9/2019 - present)

- Design an architecture that efficiently maps ML/HPC workloads on heterogeneous accelerators.
- Design and develop a runtime exception handler of AMD GPUs.
- Design a runtime exception handler of Xilinx FPGAs.

Co-op Engineer, AMD Research, Bellevue, WA (6/2020 – 9/2020, 5/2019 – 8/2019)

- Designed and developed a page migration driver for page placement policies in a tiered main memory system that contains DRAM and non-volatile memory using C on Linux.
- Designed and developed a tiered memory profiler that collects hot/cold pages.
- Developed a dynamic hugepage allocator based on system events collected by PMU.
- Profiled and analyzed CloudSuite and HPC benchmarks.
- Developed a tired memory emulation based on protection faults.

Research Assistant, NC State University, Raleigh, NC (8/2018 - 5/2019)

- Designed and developed an NVM SSD that accelerates the data preparation for a machine learning application based on TensorFlow.

Embedded Software Engineer, Telechips Inc, Korea (1/2014 - 6/2018)

- Designed and developed a RTOS driver that enables early initialization of audio for automotive environments.
- Developed inter processor communication APIs between ARM Cortex-A7 processors.

Research Assistant, Soongsil University, Korea (3/2012 - 1/2014)

- Designed and developed an Android-based motion control application.

PUBLICATIONS

[2] Jinyoung Choi, Sergey Blagodurov, and Hung-Wei Tseng. Dancing in the Dark: Profiling for Tiered Memory. 12th Annual Non-Volatile Memories Workshop (NVMW), 2021.

[1] Jinyoung Choi, Sergey Blagodurov, and Hung-Wei Tseng. Dancing in the Dark: Profiling for Tiered Memory. 35th IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2021.

ISSUED PATENTS

[2] Method and apparatus for scheduling pipeline of multiprocessor-based motion control software [US9971631].

[1] Master device for calculating synchronized actuation time of multiple slave devices and method for controlling the same [US9191294].